Method for producing a silicon single crystal having few crystal defects, and a silicon single crystal and silicon wafers produced by the method

Patent Number: EP0909840

Publication date: 1999-04-21

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Requested Patent: JP11116391

Application Number: EP19980308020 19981001

Priority Number(s): JP19970303483 19971017

IPC Classification: C30B15/00 ; C30B15/14 ; C30B29/06

EC Classification: C30B15/00+29/06 ; C30B15/14

Equivalents:

Abstract

A single crystal is grown in accordance with a Czochralski method such that the time for passing through a temperature zone of 1150-1080 DEG C is 20 minutes or less, or such that the length of a portion of the single crystal corresponding to the temperature zone of 1150-1080 DEG C in the temperature distribution is 2.0 cm or less. Alternatively, the single crystal is grown such that the time for passing through a temperature zone of 1250-1200 DEG C is 20 minutes or less, or such that the length of a portion of the single crystal corresponding to the temperature zone of 1250-1200 DEG C in the temperature distribution is 2.0 cm or less. This method decreases both the density and size of so-called grown-in defects such as FPD (100 defects/cm<2> or less), LSTD, and COP (10 defects/cm<2> or less) to thereby enable efficient production of a single crystal having an excellent good chip yield (80% or greater) in terms of oxide dielectric breakdown voltage characteristics.

Description

BACKGROUND OF THE INVENTION

Field of the Invention:

[0001] The present invention relates to a method for producing a silicon single crystal in which the silicon single crystal is pulled in accordance with the Czochralski method (hereinafter referred to as the CZ method), and which can reduce the density and size of crystal defects, called grown-in defects, generated in the crystal in the course of the pulling operation, thereby enabling production of a silicon single crystal having an excellent oxide dielectric breakdown voltage characteristics. The present invention also relates to a silicon single crystal and silicon wafers produced by the method.

Description of the Related Art:

[0002] In order to cope with an increase in the degree of fineness and the degree of integration of semiconductor circuits, quality requirements are recently becoming severer on silicon single crystals which are used as a base material. Particularly, there has been required a reduction in density and size of grown-in defects such as flow pattern defects (FPD), laser scattering tomography defects (LSTD), and crystal originated particles (COP). In order to meet such a requirement, various measures have been employed.

[0003] For example, in order to decrease the above-described defects, there may be used a technique disclosed in Japanese Patent Application Laid-Open (kokai) No. 8-337490, in which the time for passing through a temperature zone of 1150-1080 DEG C during pulling of a single crystal is increased. This technique was developed as a result of investigations and studies regarding the relationship between the thermal history of a silicon single crystal during the growth thereof and introduced crystal defects. For example, when the time for passing through the 1150-1080 DEG C temperature zone was made equal to or greater than 60 minutes, the FPD density decreased from 1000 defects/cm<2> to 400 defects/cm<2>. The good chip yield in terms of oxide-film dielectric breakdown strength which can be used as a parameter for evaluating device characteristics increased from a level below 50% to a level greater than 80%.

[0004] Meanwhile, recent studies have revealed that although the density of defects is decreased as the time for passing through the 1150-1080 DEG C temperature zone is increased, the size of the defects increases. That is, changing the length of the time for passing through the temperature zone causes only a change in the ratio between the density and size of crystal defects but does not cause a change in the total volume of the crystal defects.

[0005] The oxide dielectric breakdown voltage characteristics which can be used as a parameter for evaluating device characteristics has a strong correlation with the density of crystal defects, and a better oxide dielectric breakdown voltage characteristics is obtained when the defects are relatively large in size and low in density. Therefore, in order to improve the oxide dielectric breakdown voltage characteristics, there has been employed a measure in which the density of defects is decreased at the sacrifice of an increase in the size of the defects.

[0006] However, it recently has been reported that defects having a larger size, called COP (Crystal Originated Particles), cause adverse effects on semiconductor devices. Therefore, there has arisen a requirement for concurrently achieving reduction of the density of defects or improvement of the dielectric breakdown strength, and reduction of the size of the defects.

SUMMARY OF THE INVENTION

[0007] In view of the foregoing, an object of the invention is to establish a method of producing a single crystal, which can decrease both the density and size of so-called grown-in defects such as FPD, LSTD, and COP, to thereby enable efficient production of a single crystal having an excellent oxide dielectric breakdown voltage characteristics.

[0008] In order to achieve the above-described object, the present invention provides a method for producing a silicon single crystal in accordance with the CZ method, wherein the single crystal is grown such that the time for passing through a temperature zone of 1150-1080 DEG C is 20 minut s or less.

[0009] The inventors of the present inv ntion found that if a singl crystal being grown is rapidly cool d such that the time for passing through the 1150-1080 DEG C t mp rature zon is 20 minutes or less, there is a region where the FPD density starts to decr as due to the shortened passing time. When the tim for passing through th temperature zone is d creased, the FPD density and th defect size both decr ase, r sulting in an increase in the good chip yield in terms of oxide dielectric breakdown voltage characteristics which can be used as a parameter for evaluating device characteristics. Thus, it becomes possible to stably produce a silicon single crystal by the CZ method and the wafer, which crystal has an extremely low defect density over the entire cross section of the crystal, while maintaining high productivity.

[0010] The present invention also provides a method for producing a silicon single crystal in accordance with a CZ method, wherein the single crystal is grown such that the length of a portion of the single crystal corresponding to a temperature zone of 1150-1080 DEG C in the temperature distribution is 2.0 cm or less.

[0011] The inventors of the present invention found that if the length of the portion of the single crystal corresponding to a temperature zone of 1150-1080 DEG C in the temperature distribution becomes 2.0 cm or less, the time for passing through the 1150-1080 DEG C temperature zone is shortened even when the single crystal is grown at an ordinary pulling speed, whereby there is a region in which the FPD density starts to decrease. When the length of the portion of the single crystal corresponding to the temperature zone is decreased in order to shorten the time required for passing through the temperature zone, the FPD density and the defect size both decrease, resulting in an increase in the good chip yield in terms of oxide dielectric breakdown voltage characteristics. Thus, it becomes possible to stably produce a silicon single crystal and the wafer, which crystal has an extremely low defect density over the entire cross section of the crystal, while maintaining high productivity.

[0012] In the above-described producing methods of the present invention, the single crystal is preferably grown such that the above-described temperature zone is rapidly cooled, and the time for passing through a temperature zone of 1250-1200 DEG C is 20 minutes or less, or such that the length of a portion of the single crystal corresponding to the temperature zone of 1250-1200 DEG C in the temperature distribution is 2.0 cm or less.

[0013] That is, in the preferred producing method, the producing method by the CZ method in which a single crystal is grown such that the time for passing through the temperature zone of 1150-1080 DEG C is 20 minutes or less, or such that the length of a portion of the single crystal corresponding to the temperature zone of 1150-1080 DEG C in the temperature distribution is 2.0 cm or less, is combined with the producing method by the CZ method in which the single crystal is grown such that the time for passing through the temperature zone of 1250-1200 DEG C is 20 minutes or less, or such that the length of a portion of the single crystal corresponding to the temperature zone of 1250-1200 DEG C in the temperature distribution is 2.0 cm or less.

[0014] When a single crystal being grown is cooled rapidly such that the time for passing through the temperature zone of 1250-1200 DEG C is 20 minutes or less, or such that the length of a portion of the single crystal corresponding to the temperature zone of 1250-1200 DEG C in the temperature distribution is 2.0 cm or less, formation of crystal defect nuclei is prevented so that the FPD density decreases. Also, it was confirmed that when the time for passing through the temperature zone is shortened or when the length of the portion of the single crystal corresponding to the temperature zone is shortened, not only the number of crystal defects such as FPD but also the size of such defects decrease, resulting in an increase in the good chip yield in terms of oxide dielectric breakdown voltage characteristics (see Japanese Patent Application Laid-Open (kokai) No. 9-202684).

[0015] Therefore, when the method in which rapid cooling is performed in the temperature zone of 1250-1200 DEG C is combined with the above-described method in which rapid cooling is performed in the temperature zone of 1150-1080 DEG C, the density and size of defects can be decreased further.

[0016] That is, according to this method, both of high and low temperature zones are cooled rapidly, so that the time for passing these temperature zones becomes short enough to prevent coagulation and growth of crystal defects, and formation of crystal defect nuclei themselves can be suppressed. In this manner, the synergetic effect of the two-stage rapid cooling further decreases the density and size of defects such as FPD, so that the good chip yield in terms of oxide dielectric breakdown voltage characteristics can be increased.

[0017] The present invention also provides a silicon crystal produced in accordance with one of the producing methods of the present invention.

[0018] When the above-described rapid cooling method which has not conventionally been practic d is applied to crystal growth, not only the density of crystal defects such as FPD but also the size of such defects d creas , so that there can be obtained a silicon single crystal having an increased good chip yield in terms of oxide dielectric breakdown voltage characteristics of wafers obtain d from the crystal.

[0019] Th present invention further provides a silicon wafer whose FPD density is not greater than 100 def cts/cm<2>, whose good chip yield in terms of oxide dielectric breakdown voltage characteristics is 80% or greater, and whose COP density is not greater than 10 defects/cm<2>.

[0020] In this way, when silicon wafers are sliced from the silicon crystal produced in accordance with on or the producing methods of the present invention and are then mirror-polished, wafers having an extremely low defect density and an excellent characteristic in terms of oxide dielectric breakdown voltage characteristics can be produced at a high yield.

[0021] As described above, when a single crystal is produced in accordance with the CZ method, the temperature zone of 1150-1080 DEG C and/or the temperature zone of 1250-1200 DEG C are cooled rapidly. Therefore, it is possible to produce high quality wafers in which the density of FPD is not greater than 100 defects/cm<2>, the density of COP is not greater than 10 defects/cm<2>, and the size of defects is extremely small, and whose good chip yield in terms of oxide dielectric breakdown voltage characteristics is 80% or greater. In addition, since the operation of pulling a single crystal can be performed while a high pulling speed is maintained, high quality crystals can be produced with high productivity.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a graph showing the relationship between the speed of passing through a crystal rapid-cooling temperature zone and the density of FPD defects of resultant wafers;
FIG. 2 is a graph showing the relationship between the speed of passing through a crystal rapid-cooling temperature zone and the good chip yield of resultant wafers in terms of C-mode oxide dielectric breakdown voltage characteristics;
FIG. 3 is a schematic view showing the structure of a rapid-cooling type silicon single crystal pulling apparatus used in the present invention;
FIG. 4 is a schematic view showing the structure of a conventional gradual-cooling type silicon single crystal pulling apparatus; and
FIG. 5 is a schematic view showing the structure of a conventional silicon single crystal pulling apparatus.

DESCRIPTION OF THE INVENTION AND THE PREFERRED EMBODIMENTS

[0023] The present invention will now be described in detail, but the present invention is not limited thereto.

[0024] The inventors of the present invention found that in order to decrease both the density and size of various defects generated in a single crystal being pulled, it is effective to shorten the time for passing through a specific temperature zone or to shorten the length of a portion of the crystal corresponding to the specific temperature zone, i.e., to cause the crystal to have a thermal history such that the specific temperature zone is cooled rapidly. Based on this finding and through detailed investigations on various operating conditions, the present invention was completed.

[0025] First, terms appearing herein will be described.

1) FPD (Flow Pattern Defect) denotes flow patterns which, together with pits, are generated in the surface of a wafer which is sliced from a grown silicon single-crystal ingot and which is treated by the steps of: removing a damaged layer from the surface portion of the wafer through etching with a mixed solution of hydrofluoric acid and nitric acid; and etching the wafer surface with a mixed solution of K2Cr2O7, hydrofluoric acid, and water (Secco etching). As FPD density in the wafer surface portion becomes higher, failure rate with regard to dielectric breakdown strength of oxide film increase (Japanese Patent Laid-Open (kokai) No. 4-192345).
2) LSTD (Laser Scattering Tomography Defect) denotes a defect existing in a wafer, and the scattering light due to the defect can be detected in the following manner. In that, a wafer is sliced from a grown silicon single-crystal ingot, and is then treated by the steps of: removing a damaged layer from the surface portion of the wafer through etching with a mixed solution of hydrofluoric acid and nitric acid; and cleaving the wafer. When infrared light is introduced into the wafer through the cleavage plane, and light exiting from the wafer surface is detected, a scattering light due to the defects existing in a wafer can be detected. A scattering defect detected in this observation has already been reported at a meeting of an academic

society or the like and is considered to be an oxide precipitate (J.J.A.P. vol. 32, p.3679, 1993). According to r cent research, LSTD is reported to be an octahedral void.
3) COP (Crystal Originated Particle) denotes a defect which deteriorates the dielectric breakdown strength of oxid film a a central portion of a wafer and which is revealed as FPD in the case of treatment through Secco etching, but is revealed as COP in the case of cleaning in SC-1 (cleaning by using mixed aqueous solution of ammonia, hydrogen peroxide, example of ratio is NH4OH:H2O2:H2O = 1:1:10) which serves as a selective etchant. The pit has a diameter not greater than 1 mu m and is examined by a light scattering method.

[0026] Since the density of defects such as FPD, LSTD, and COP has a correlation with the failure rate in terms of oxide dielectric breakdown voltage characteristics, these kinds of defects are all considered factors that degrade the oxide dielectric breakdown voltage characteristics. Accordingly, the FPD, LSTD, and COP must be reduced in order to improve the oxide dielectric breakdown voltage characteristics of a silicon single crystal produced in accordance with the CZ method.

[0027] The inventors of the present invention first conducted studies in order to reduce the size of defects. As a result, the inventors judged that coagulation of defects certainly occurs in the temperature zone of 1150-1080 DEG C, and therefore if no time is given to defects to coagulate, the size of the defects can be reduced; and that such agglomeration of defects can be prevented through shortening the time for passing through the temperature zone of 1150-1080 DEG C which time has conventionally been set to 60 minutes or longer for gradual cooling. However, it is apparent that the mere change of the passing time causes an increase in the density of crystal defects and a degradation in the oxide dielectric breakdown voltage characteristics.

[0028] In view of the foregoing, the inventors of the present invention established a hypothesis. The present inventors considered that when FPD, LSTD, and COP are detected, atomic level point defects are not observed but a group of defects having a relatively large size is detected. That is, there conceivably exists a lower limit for detection of FPD, LSTD, and COP. Therefore, if the speed of cooling a single crystal is made faster than that in the conventional method to thereby decrease the size of defects to a certain level or smaller, the size of FPD, LSTD, COP, etc. becomes very small, so that the detected density decreases and the oxide dielectric breakdown voltage characteristics can be improved.

[0029] In order to confirm the above-described hypothesis, the inventors of the present invention performed the following experiment and investigated the relationship between the time for passing through a temperature zone of 1150-1080 DEG C and the density of defects, as well as the relationship between the time for passing through the temperature zone of 1150-1080 DEG C and the oxide dielectric breakdown voltage characteristics in various cooling methods including a rapid cooling method that has not conventionally been employed. That is, a silicon single crystal was separated from silicon melt in the course of growth thereof, and pulled upward such that the crystal passed through the temperature zone of 1150-1080 DEG C at a certain passing speed. A plurality of silicon single crystals were grown in the above-described manner while the passing speed was changed in order to change the speed of cooling the silicon single crystal. FIGS. 1 and 2 show the results of this experiment.

[0030] The temperature distribution within a crystal growing apparatus used in the experiment was measured in advance, and it was confirmed that the temperature zone of 1150-1080 DEG C had a length of approximately 8 cm.

[0031] FIG. 1 shows the relationship between the speed at which a crystal passes through the temperature zone of 1150-1080 DEG C and the density of FPD. When the passing speed is not greater than 4 mm/min, i.e., when the time for passing through the temperature zone of 1150-1080 DEG C exceeds 20 minutes (the left half of FIG. 1), the FPD density increases with increasing the passing speed. By contrast, when the time for passing through the temperature zone of 1150-1080 DEG C is not greater than 20 minutes (the right half of FIG. 1), the FPD density decreases with increasing passing speed. Through the investigation and experiment performed in this time, it was found that in the hatched region the size of FPD is small and the density of FPD is low.

[0032] This phenomenon conceivably occurs because the size of defects becomes very small due to extremely rapid cooling, so that the number of defects having sizes below the detection lower limit increases.

[0033] FIG. 2 shows the relationship between the speed of passing through rapid cooling temperature zone of a crystal and the good chip yield ratio in terms of the oxide dielectric breakdown voltage characteristics. When the passing speed is decreased or increased from 4 mm/min, the good chip yield increases drastically. This graph indicates that the oxide dielectric breakdown voltage characteristics can be improved through increase of the speed of cooling such that each portion of the crystal passes through the temperature zone of 1150-1080 DEG C within 20 minutes.

[0034] Further, the present inventors found that, when the speed at which each portion of a silicon single crystal passes through the temperature zone of 1150-1080 DEG C is increas d to 8 mm/minute or greater, i.e., when the time for passing through the temperature zone of 1150-1080 DEG C is shortened to 10 minutes or less, the size of defects generated in the silicon single crystal is further reduced, so that there can be obtained a silicon single crystal having an excellent oxide dielectric breakdown voltage characteristics and a low defect crystal in which the FPD density is not greater than 100 defects/cm<2> and the good chip yield in terms of oxide dielectric breakdown voltage characteristics is 90% or more.

[0035] However, there exist cases where a single crystal cannot be grown at a speed equal to or greater than 4 mm/minute or 8 mm/min. In such cases, the inside structure of a furnace of a crystal growing apparatus may be adjusted such that the length of a portion corresponding to the temperature zone of 1150-1080 DEG C is made 2.0 cm or less. If the length of the portion of the single crystal corresponding to the temperature zone of 1150-1080 DEG C is made 2.0 cm or less, the time for passing through the 1150-1080 DEG C temperature zone can be shortened to 20 minutes or less, even when the single crystal is grown at an ordinary pulling speed. Thus, the density and size of crystal defects can be decreased to a desired level.

[0036] The inventors of the present invention had previously investigated another relationship between the thermal history of a crystal and crystal defects generated therein, which are described in Japanese Patent Application No. 8-26021 (Japanese Patent Application Laid-Open (kokai) No. 9-202684). From the investigation, the inventors had found that the time for passing through a temperature zone of 1250-1200 DEG C affects formation of crystal defect nuclei, and thus confirmed that in the temperature zone of 1250-1200 DEG C, formation of crystal defect nuclei can be suppressed when the time for passing through this temperature zone is shortened to not greater than 20 minutes.

[0037] Therefore, when the method in which the rapid cooling is performed in the temperature zone of 1150-1080 DEG C is combined with the method in which the rapid cooling is performed in the temperature zone of 1250-1200 DEG C, the formation of crystal defect nuclei is suppressed effectively, so that the density and size of defects can be decreased further.

[0038] However, there exist cases where the time for passing through a temperature zone of 1250-1200 DEG C cannot be shortened to not greater than 20 minutes through a mere increase in the crystal growth rate. In such cases, the length of a portion corresponding to the temperature zone of 1250-1200 DEG C is made 2.0 cm or less. If the length of the portion of the single crystal corresponding to the temperature zone of 1250-1200 DEG C is made 2.0 cm or less, the time for passing through the 1250-1200 DEG C temperature zone can be shortened to 20 minutes or less, even when the single crystal is grown at an ordinary pulling speed. Thus, formation of crystal defect nuclei is suppressed, and the density and size of crystal defects can be decreased to a desired level.

[0039] Embodiments of the present invention will now be described in detail with reference to the drawings. FIG. 3 shows a rapid-cooling type crystal pulling apparatus used in the present invention which operates in accordance with the CZ method. As shown in FIG. 3, the crystal pulling apparatus 30 includes a pull chamber 31, a crucible 32 provided within the pull chamber 31, a heater 34 disposed around the crucible 32, a crucible-holding shaft 33 for rotating the crucible 32 and a rotation mechanism (not shown) for rotating the crucible-holding shaft 33, a seed chuck 6 for holding a silicon seed crystal 5, a cable 7 for pulling the seed chuck 6, and a winding mechanism (not shown) for rotating or winding up the cable 7. The crucible 32 includes an inner quartz crucible for containing a silicon melt 2 and an outer graphite crucible located outside the quartz crucible. A heat insulating cylinder 35 is disposed around the heater 34.

[0040] In order to establish operating conditions for the producing method of the present invention, an annular solid-liquid interface insulator 9 is arranged around the solid-liquid interface of a single crystal such that the insulator 9 extends from the outer periphery of the solid-liquid interface to the ceiling of the pulling chamber. A gap of a few centimeters is formed between the lower end of the insulator 9 and the surface 3 of the silicon melt 2, thereby heat dissipation can be suppressed around the interface. Further, the wall thickness of the insulator 9 is gradually decreased toward the ceiling so that the gap between the insulator 9 and the single crystal 1 being grown continuously increases toward the ceiling, thereby rapid cooling can be performed. Moreover, an upper insulator 8 is provided above the heater in order to block radiant heat from the heater.

[0041] Recently, a so-called MCZ method has often been employed. When the MCZ is employed, an unillustrated magnet is disposed outside the pull chamber 31 in a horizontal direction so as to apply a magnetic field to the silicon melt 2 in a horizontal or vertical direction or in a like direction. Through the application of a magnetic field to the silicon melt 2, convection of the melt 2 is suppressed to thereby stably grow a single crystal.

[0042] Next will be described a method for growing a single crystal through use of the crystal pulling apparatus 30 of FIG. 3. First, a high-purity polycrystalline material of silicon is heated to its melting point (approximately 1420 DEG C) or higher and is thus melted in the crucible 32. Next, the cable 7 is released

until a tip end of the seed crystal 5 comes into contact with the surface of the melt 2 at a central portion or is immersed into th melt 2 at a central portion. Subsequently, the crucible-holding shaft 33 is rotat d in an appropriate direction. At the same tim , the cable 7 is rotated and wound up to thereby pull th se d crystal 5. Thus is started the growth of a single crystal. Then, through adequate regulation of the pull rat and temperature, a substantially cylindrical single-crystal ingot 1 can be obtained.

[0043] To achieve the objects of the present invention, the invention employs the following structural features. As shown in FIG. 3, the annular solid-liquid interface insulator 9 is disposed in the pull chamber 31 such that the solid-liquid interface insulator 9 surrounds the single crystal 1 and extends from a point in the vicinity of the surface of the melt to the ceiling of the pulling chamber. In addition, the upper insulator 8 is disposed above the heater 34. Further, when needed, a crystal-cooling device, for example, an unillustrated gas flow guide cylinder, may be provided above the insulator. A cooling gas is blown through the gas flow guide cylinder from above to thereby cool the single crystal 1. The gas flow guide cylinder may include a radiant heat reflector attached to a lower portion of the flow regulation tube.

[0044] As mentioned above, an insulator is arranged immediately above the surface of the melt with a predetermined gap formed therebetween, and the insulator has a structure to provide a clearance between a single crystal being grown and the upper portion of the insulator such that the clearance continuously increases upward. This structure yields a heat keeping effect in the vicinity of the crystal growth interface due to the radiant heat. At the upper portion of the insulator, cooling is effected rapidly in a specific temperature zone. In addition, an upper portion of the crystal is shielded from radiant heat from the heat r or the like. As a result, the operating conditions for the producing method of the present invention are established in cooperation with control of the pulling speed of the crystal.

[0045] In addition to the gas flow guide cylinder, an air-cooled duct, a water-cooled tube, or a like device may be provided as a crystal cooling device, such that the device surrounds a crystal being grown so as to establish a desired temperature gradient in the crystal.

[0046] For comparison with the rapid cooling type crystal pulling apparatus used in the present invention, a conventional gradual-cooling type silicon single crystal pulling apparatus is shown in FIG. 4, and a conventional silicon single crystal pulling apparatus is shown in FIG. 5. Their basic structures are the same as that of the rapid cooling type crystal pulling apparatus used in the present invention (see FIG. 3). However, the apparatus shown in FIGS. 4 and 5 differ from the apparatus used in the present invention in terms of the presence/absence of the solid-liquid interface insulator and the upper insulator above the heater, and the position of the insulator.

EXAMPLES

[0047] The present invention will next be described by way of examples, which should not be construed as limiting the invention.

Example 1:

[0048] A silicon single crystal was pulled through use of the crystal producing apparatus 30 shown in FIG. 3, whose furnace has a structure adapted to rapid cooling. Forty kg of polycrystalline material of silicon were charged into a quartz crucible having a diameter of 18 inches. A single crystal ingot having a diameter of 6 inches and orientation <100> was pulled in accordance with the CZ method.

[0049] The pulling of the single crystal ingot was performed under preset growth conditions such that the time for passing through the 1150-1080 DEG C temperature zone was 12 minutes, the length of the 1150-1080 DEG C temperature zone was 2.0 cm, and the speed of passing through the 1150-1080 DEG C temperature zone (crystal pulling speed) was 1.67 mm/min.

[0050] Wafers were sliced from the thus-obtained single crystal ingot. The wafers were mirror-polished, yielding single-crystal mirror wafers of silicon. The thus-obtained mirror wafers were measured in order to determine the grown-in defects and the oxide dielectric breakdown voltage characteristics (C-mode). Table 1 shows the values of thus determined FPD, COP, and TZDB (Time Zero Dielectric Breakdown) [good chip yield in terms of oxide dielectric breakdown voltage characteristics].

[0051] The oxide dielectric breakdown voltage characteristics (C-mode) was measured under the conditions such that the thickness of oxide film was 25 nm, measurement electrodes were phosphorous-doped polysilicon, the area of the electrodes was 8 mm<2>, and current employed for judgment was 1 mA/cm<2>, and a chip that did not cause dielectric breakdown in an electric field of 8 MV/cm or below was judged to be good.

Exampl 2:

[0052] A single crystal ingot was pulled under the same conditions and through use of the same apparatus as that used in Example 1, except that the pulling conditions were set such that the time for passing through the 1250-1200 DEG C temperature zone was 12 minutes, the length of the 1250-1200 DEG C temperature zone was 2.0 cm, and the speed of passing through the 1250-1200 DEG C temperature zone (crystal pulling speed) was 1.67 mm/min. The resultant values of thus obtained silicon wafer's FPD, COP, and TZDB are also shown in Table 1.

Comparative Example 1:

[0053] A single crystal ingot was pulled at a pulling speed of 1.1 mm/min through use of the crystal pulling apparatus 40 shown in FIG. 4, whose furnace has a structure adapted to gradual cooling in the temperature zone of 1150-1080 DEG C. Subsequently, mirror-polished wafers were produced from the thus-grown ingot and were measured in the same manner as in Example 1. The results of the measurement are also shown in Table 1.

[0054] The crystal pulling apparatus 40 shown in FIG. 4 has basically the same structure as that of the crystal pulling apparatus 30 used in Examples 1 and 2. However, in order to effect gradual cooling in the temperature zone of 1150-1080 DEG C, a heat insulating cylinder 35 surrounding a heater 34 is extended upward, and a carbon ring 11 is placed thereon in order to prevent radiation of radiant heat from the crystal surface, thereby decreasing the cooling speed. Further, a part of the heat insulating cylinder 35 surrounding the heater 34 is cut away in order to provide a split portion 10 to thereby divide the heat insulating cylinder 35 into upper and lower portions. Thus, the high temperature zone between the melting point and 1200 DEG C is cooled rapidly. The furnace having the above-described structure decreases the time for passing through the high temperature zone and increases the time for passing through the temperature zone of 1150-1080 DEG C in comparison with the conventional rapid cooling method in Comparative Example 2.

Comparative Example 2:

[0055] A single crystal ingot was pulled at a pulling speed of 1.25 mm/min through use of the crystal pulling apparatus 50 shown in FIG. 5, whose furnace has a conventional structure. Another pulling conditions were not set. In this case, no cooling device was disposed in the pulling apparatus. Subsequently, mirror-polished wafers were produced from the thus-grown ingot and were measured in the same manner as in Example 1. The results of the measurement are also shown in Table 1.

[0056] The present invention is not limited to the above-described embodiments. The above-described embodiments are mere examples, and those having the substantially same structure as that described in the appended claims and providing the similar action and effects are Included in the scope of the present invention.

Claims

1. A m thod for producing a silicon singl crystal in accordance with a Czochralski method, characterized in that the singl crystal is grown in such that the time for passing through a temperature zone of 1150-1080 DEG C is 20 minutes or less.

2. A method for producing a silicon single crystal in accordance with a Czochralski method, characterized in that the single crystal is grown such that the length of a portion of the single crystal corresponding to a temperature zone of 1150-1080 DEG C in the temperature distribution is 2.0 cm or less.

3. A method for producing a silicon single crystal according to Claim 1 or 2, characterized in that the single crystal is grown such that the time for passing through a temperature zone of 1250-1200 DEG C is 20 minutes or less.

4. A method for producing a silicon single crystal according to Claim 1 or 2, characterized in that the singl crystal is grown such that the length of a portion of the single crystal corresponding to a temperature zon of 1250-1200 DEG C in the temperature distribution is 2.0 cm or less.

5. A silicon crystal produced in accordance with the method according to any one of Claims 1 - 4.

6. A silicon wafer whose FPD density is not greater than 100 defects/cm<2>, whose good chip yield in terms of oxide dielectric breakdown voltage characteristics is 80% or greater, and whose COP density is not greater than 10 defects/cm<2>.

FIG. 1

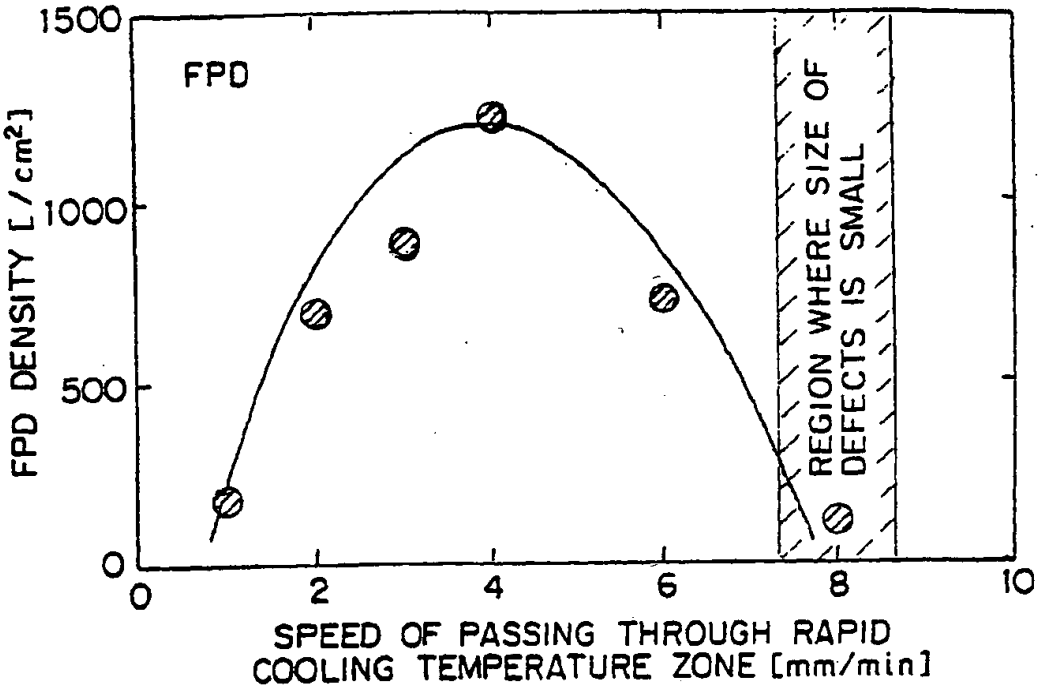

FPD
FPD DENSITY [/cm²]
1500
1000
500
0
0
2
4
6
8
10
REGION WHERE SIZE OF DEFECTS IS SMALL
SPEED OF PASSING THROUGH RAPID COOLING TEMPERATURE ZONE [mm/min]

FIG. 2

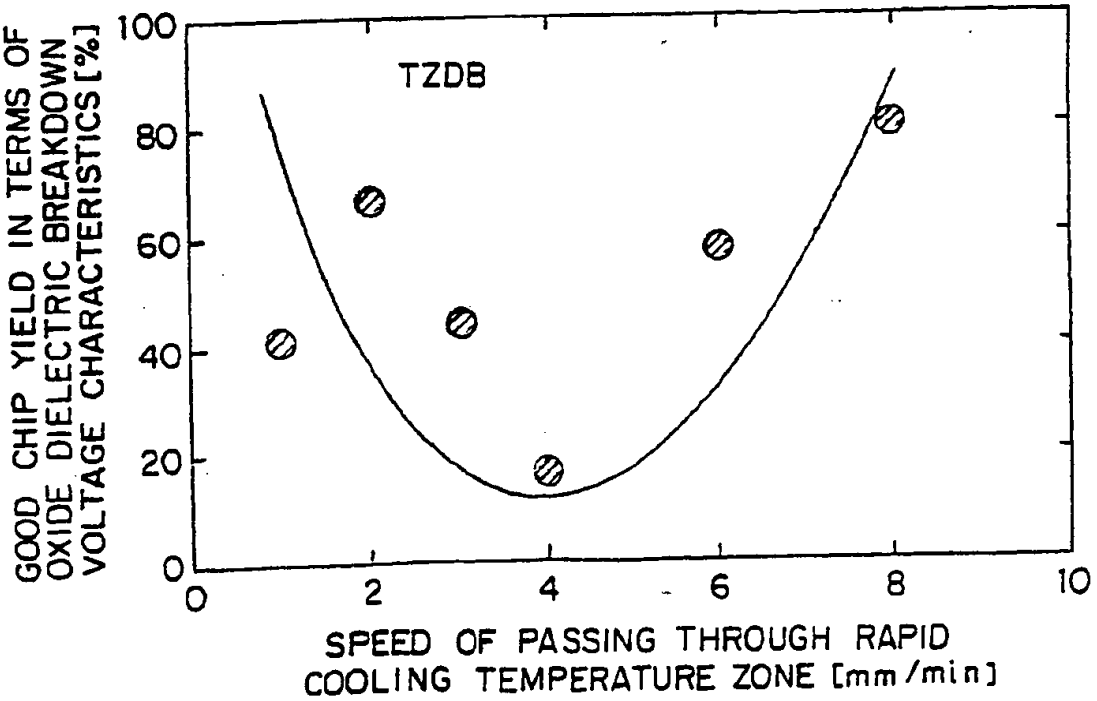

TZDB
GOOD CHIP YIELD IN TERMS OF OXIDE DIELECTRIC BREAKDOWN VOLTAGE CHARACTERISTICS [%]
100
80
60
40
20
0
0
2
4
6
8
10
SPEED OF PASSING THROUGH RAPID COOLING TEMPERATURE ZONE [mm/min]

FIG. 3

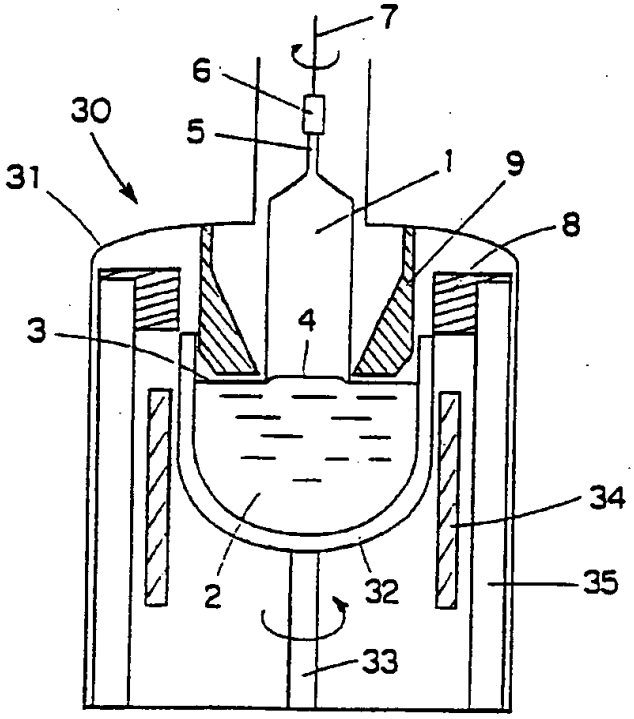


FIG. 4

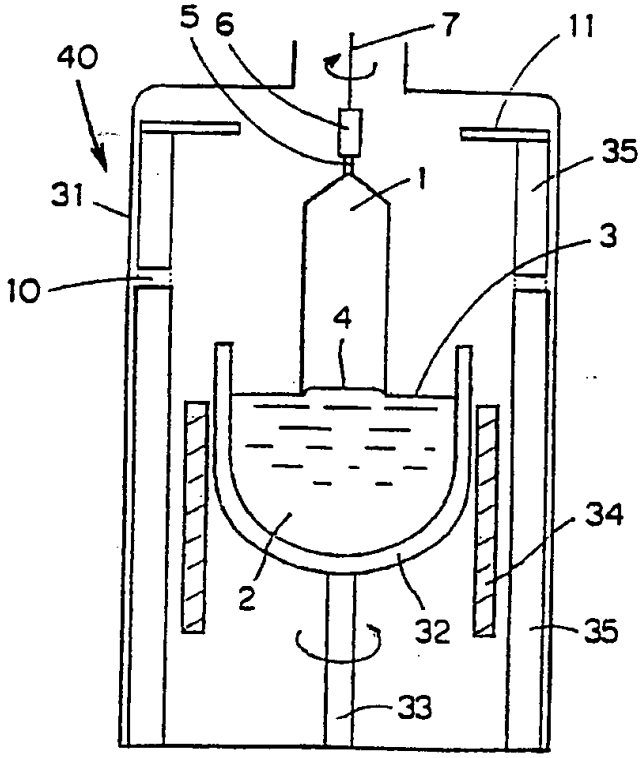
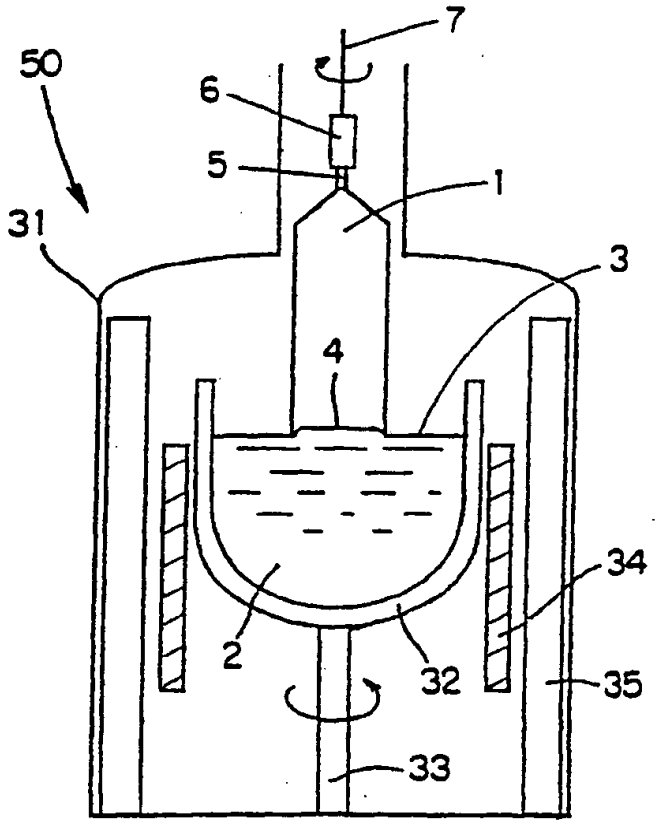


FIG. 5



(19)日本国特許庁（ＪＰ）　(12)公開特許公報（Ａ）　(11)特許出願公開番号

特開平11－116391

(43)公開日　平成11年(1999)４月27日

(51)Int.Cl.[6]	識別記号	ＦＩ	
Ｃ３０Ｂ　29/06	５０２	Ｃ３０Ｂ　29/06	５０２Ｊ
15/20		15/20	

審査請求　未請求　請求項の数６　ＦＤ　（全８頁）

(21)出願番号　特願平9－303483

(22)出願日　平成９年(1997)10月17日

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最終頁に続く

(54)【発明の名称】　結晶欠陥の少ないシリコン単結晶の製造方法ならびにこの方法で製造されたシリコン単結晶およびシリコンウエーハ

(57)【要約】　（修正有）

【課題】　ＦＰＤ（１００ケ／ｃｍ^2 以下）、ＬＳＴＤ、ＣＯＰ（１０ケ／ｃｍ^2 以下）等のグローンイン欠陥と呼ばれる欠陥の密度とサイズの同時低減を行い、酸化膜耐圧特性良品率（８０％以上）に優れたシリコン単結晶及びウエーハを高生産性で作製する製造方法を確立する。

【解決手段】　ＣＺ法による結晶成長時に、１１５０～１０８０℃の温度域の通過時間を２０分以下にする、または結晶の温度分布の内１１５０～１０８０℃の温度域に相当する部分の長さを２．０ｃｍ以下とするシリコン単結晶の製造方法、或は、さらに結晶成長時に、１２５０～１２００℃の温度域の通過時間を２０分以下にする、または結晶の温度分布の内１２５０～１２００℃の温度域に相当する部分の長さを２．０ｃｍ以下にするシリコン単結晶の製造方法。

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【特許請求の範囲】

【請求項１】　チョクラルスキー法によって単結晶を製造する場合において、育成されるシリコン単結晶が結晶成長時に、１１５０～１０８０℃の温度域の通過時間が２０分以下となるようにすることを特徴とするシリコン単結晶の製造方法。

【請求項２】　チョクラルスキー法によって単結晶を製造する場合において、育成されるシリコン単結晶が結晶成長時に、結晶の温度分布の内、１１５０～１０８０℃の温度域に相当する部分の長さを２．０ｃｍ以下にすることを特徴とするシリコン単結晶の製造方法。

【請求項３】　チョクラルスキー法によって単結晶を製造する場合において、育成されるシリコン単結晶が結晶成長時に、１２５０～１２００℃の温度域の通過時間が２０分以下となるようにすることを特徴とする請求項１または請求項２に記載のシリコン単結晶の製造方法。

【請求項４】　チョクラルスキー法によって単結晶を製造する場合において、育成されるシリコン単結晶が結晶成長時に、結晶の温度分布の内、１２５０～１２００℃の温度域に相当する部分の長さを２．０ｃｍ以下にすることを特徴とする請求項１または請求項２に記載のシリコン単結晶の製造方法。

【請求項５】　請求項１～請求項４のいずれか１項に記載した方法によって製造されたシリコン単結晶。

【請求項６】　ＦＰＤ密度が１００ケ／ｃｍ^2 以下であり、酸化膜耐圧特性が８０％以上であり、かつＣＯＰ密度が１０ケ／ｃｍ^2 以下であることを特徴とするシリコンウエーハ。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、チョクラルスキー法（以下、ＣＺ法という）によってシリコン単結晶を引上げる際に、結晶内部に存在するグローンイン（Ｇｒｏｗｎ－ｉｎ）欠陥と呼ばれる結晶欠陥の密度とサイズが小さく、酸化膜耐圧特性に優れた単結晶を製造する方法、並びにこの方法で製造されたシリコン単結晶とシリコンウエーハに関する。

【０００２】

【従来の技術】近年、半導体回路の微細化、高集積化に伴い、そのベースとなるシリコン単結晶に対する品質要求も厳しくなってきている。特に、ＦＰＤ、ＬＳＴＤ、ＣＯＰ等のいわゆるグローンイン欠陥と呼ばれる欠陥の密度とサイズの同時低減が要求されており、種々の対応がなされている。

【０００３】これら欠陥の低減方法としては、例えば特開平８－３３７４９０号公報にあるように、結晶引上げ中の１１５０～１０８０℃の温度域を通過する時間を長くするという方法がある。これはシリコン単結晶成長時に、単結晶が受けた熱履歴と、導入された結晶欠陥との関係を種々調査、検討した結果開発された手法で、例えば、１１５０～１０８０℃の温度域を通過する時間を６０分以上にすることにより、ＦＰＤ密度がもともと１０００ケ／ｃｍ^2 以上あったものが４００ケ／ｃｍ^2 にまで改善されている。また、デバイス特性に近い評価をすることができる酸化膜耐圧特性の良品率では５０％以下から８０％以上にまで向上した。

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【０００４】

【発明が解決しようとする課題】ところで、最近の研究では、１１５０～１０８０℃の温度域を通過する時間を長くすればする程、結晶欠陥の密度は減らせても、そのサイズは拡大することが判ってきた。すなわち、この温度帯を通過する時間の長短は、結晶欠陥のトータルな体積は変化せず、密度とサイズの比を変化させるだけということが判ってきた。

【０００５】ただし、デバイス特性に近い評価が可能な酸化膜耐圧特性はこれら欠陥の密度との相関関係が強く、サイズが大きくて密度の小さな方が酸化膜耐圧特性も良好となる。そこで、酸化膜耐圧特性向上のためには、欠陥のサイズ拡大を犠牲にしても密度を減らすという策を採ってきた。ところが、最近ではＣＯＰと呼ばれるよりサイズの大きい欠陥のデバイスへの悪影響が報告されており、欠陥の密度低減つまり耐圧の向上と共にサイズの低減も行う必要が生じてきた。

【０００６】従って、本発明が解決しようとする課題は、特に、ＦＰＤ、ＬＳＴＤ、ＣＯＰ等のグローンイン欠陥と呼ばれる欠陥の密度とサイズの同時低減を行い、酸化膜耐圧特性に優れた単結晶を高生産性で作製する製造方法を確立することを主たる目的とする。

【０００７】

【課題を解決するための手段】上記課題を解決するため、本発明の請求項１に記載した発明は、ＣＺ法によって単結晶を製造する場合において、育成されるシリコン単結晶が結晶成長時に、１１５０～１０８０℃の温度域の通過時間が２０分以下となるようにすることを特徴とするシリコン単結晶の製造方法である。

【０００８】このように、１１５０～１０８０℃の温度域の通過時間を２０分以下となるように急冷すると、通過時間の短縮に伴ってＦＰＤ密度が減少に転じる領域があることを見出した。そして、該温度域の通過時間を短縮して行くと、ＦＰＤ密度が減少するとともに欠陥サイズも小さくなり、デバイス特性に近い評価をすることができる酸化膜耐圧特性の良品率も向上し、結晶全面にわたって極低欠陥密度であるＣＺ法によるシリコン単結晶及びウエーハを安定して高生産性を維持しながら製造することができる。

【０００９】本発明の請求項２に記載した発明は、ＣＺ法によって単結晶を製造する場合において、育成されるシリコン単結晶が結晶成長時に、結晶の温度分布の内、１１５０～１０８０℃の温度域に相当する部分の長さを２．０ｃｍ以下にすることを特徴とするシリコン単結晶

の製造方法である。

【0010】このように、成長中の結晶の温度分布の内、1150～1080℃の温度域に相当する部分の長さを2．0cm以下となるようにすると、たとえ通常の引上げ速度で結晶を成長させても、この温度域を通過する時間が短縮され、これに伴ってFPD密度が減少に転じる領域があることを見出し、またこの温度域の長さを短縮する、すなわち通過時間を短縮すると、FPD密度の減少と共に欠陥サイズも小さくなり、酸化膜耐圧特性の良品率も向上し、結晶全面にわたって極低欠陥密度であるシリコン単結晶及びウエーハを安定して高生産性を維持しながら製造することができる。

【0011】本発明の請求項3に記載した発明は、CZ法によって単結晶を製造する場合において、育成されるシリコン単結晶が結晶成長時に、上記温度域を急冷するとともに、1250～1200℃の温度域の通過時間が20分以下となるようにした。また、本発明の請求項4では、結晶の温度分布の内、1250～1200℃の温度域に相当する部分の長さを2．0cm以下になるようにした。

【0012】この製法は、CZ法によって単結晶を製造する場合において、育成されるシリコン単結晶が結晶成長時に、1150～1080℃の温度域の通過時間が20分以下となるように、あるいは、結晶の温度分布の内、1150～1080℃の温度域に相当する部分の長さが2．0cm以下になるように急冷する製法と、1250～1200℃の温度域の通過時間が20分以下、あるいは、結晶の温度分布の内、1250～1200℃の温度域に相当する部分の長さを2．0cm以下となるように急冷する製法とを組合せたことを特徴とするシリコン単結晶の製造方法である。

【0013】このよう、育成されるシリコン単結晶が結晶成長時に、1250～1200℃の温度域の通過時間が20分以下となるように急冷するか、あるいは、結晶の温度分布の内、1250～1200℃の温度域に相当する部分の長さを2．0cm以下となるように急冷すると、結晶欠陥核の形成が阻害されるためにFPD密度が減少する。また、シリコン単結晶の該温度域の通過時間を短縮するか、あるいは該温度域長さを短くすると、FPD密度等の結晶欠陥の減少のみならず欠陥サイズも小さくなり、酸化膜耐圧特性の良品率も向上することが確認されている（特開平9－202684号参照）。

【0014】そこで、これと前記1150～1080℃の温度域を急冷する方法とを組み合わせれば、より一層欠陥密度、欠陥サイズを小さくすることが可能となる。すなわち、この製法によれば、高温域と中温域との二段階の温度帯域をともに急冷することにより、結晶欠陥が凝集及び成長する時間がなくなるとともに、結晶欠陥核の形成そのものを抑制でき、二段階の相乗効果によって一層FPD等の結晶欠陥密度の減少と共に欠陥サイズを小さくすることができ、酸化膜耐圧特性の良品率もさらに向上するというものである。

【0015】本発明の請求項5に記載した発明は、請求項1～請求項4のいずれか1項に記載したシリコン単結晶の製造方法によって製造されたシリコン単結晶である。このように、従来実施されたことのない急冷法を成長結晶に適用すれば、FPD等の結晶欠陥密度の減少と共に欠陥サイズも小さくなり、ウエーハの酸化膜耐圧特性の良品率も向上したシリコン単結晶が得られる。

【0016】本発明の請求項6に記載した発明は、FPD密度が100ケ／cm^2 以下であり、酸化膜耐圧特性が80%以上であり、かつCOP密度が10ケ／cm^2 以下であることを特徴とするシリコンウエーハである。このように、前記請求項1～4で作製したシリコン単結晶からシリコンウエーハを切り出し、鏡面研磨すると、極低欠陥密度で酸化膜耐圧特性に優れたウエーハを高収率で得ることができる。

【0017】以下、本発明についてさらに詳述するが、本発明はこれらに限定されるものではない。本発明者らは、単結晶製造時の引上げ結晶内に発生する諸欠陥の密度を低減し、しかもそのサイズを小さくするには、特定温度域の通過時間を短くする、あるいは、特定温度域の結晶長さを短くする、すなわち成長結晶の熱履歴として所定の温度域を急冷すれば有効であることを見出し、諸条件を精査して本発明を完成させたものである。

【0018】先ず、本発明で使用される各用語について予め解説しておく。

1）FPD（Flow Pattern Defect）とは、成長後のシリコン単結晶棒からウェーハを切り出し、表面の歪み層を弗酸と硝酸の混合液でエッチングして取り除いた後、$K_2Cr_2O_7$ と弗酸と水の混合液で表面をエッチング（Seccoエッチング）することによりピットおよびさざ波模様が生じる。このさざ波模様をFPDと称し、ウェーハ面内のFPD密度が高いほど酸化膜耐圧の不良が増える（特開平4－192345号公報参照）。

【0019】2）LSTD（Laser Scattering Tomography Defect）とは、成長後のシリコン単結晶棒からウエーハを切り出し、表面の歪み層を弗酸と硝酸の混合液でエッチングして取り除いた後、ウエーハを劈開する。この劈開面より赤外光を入射し、ウエーハ表面から出た光を検出することでウエーハ内に存在する欠陥による散乱光を検出することができる。ここで観察される散乱体については学会等ですでに報告があり、酸素析出物とみなされている（J．J．A．P．　Vol．32，P3679，1993参照）。また、最近の研究では、八面体のボイド（穴）であるという結果も報告されている。

【0020】3）COP（Crystal Originated Particle）とは、ウエーハの中心

部の酸化膜耐圧を劣化させる原因となる欠陥で、ＳｅｃｃｏエッチではＦＰＤになる欠陥が、ＳＣ－１洗浄（$NH_4OH:H_2O_2:H_2O=1:1:10$の混合液による洗浄）では選択エッチング液として働き、ＣＯＰになる。このピットの直径は１μｍ以下で光散乱法で調べる。

【００２１】これらＦＰＤ、ＬＳＴＤ、ＣＯＰ等の欠陥密度は酸化膜耐圧の不良率と相関があることから、共に酸化膜耐圧劣化因子と考えられている。従って、ＣＺ法によりシリコン単結晶の酸化膜耐圧を改善させるためには、これらＦＰＤ、ＬＳＴＤ、ＣＯＰ等を減少させる必要がある。

【００２２】本発明者等は、先ず第１に欠陥のサイズを小さくすることを考えて調査した。その結果、上記したように１１５０～１０８０℃の温度域では欠陥の凝集が起こっていることは間違いなく、欠陥が凝集する時間を与えなければ、欠陥のサイズの低減は可能であり、それには１１５０～１０８０℃の温度域の通過時間を従来は６０分以上にして徐冷していたのとは逆に短縮すれば実現可能であると判断した。しかし、通過時間だけ変えたのでは、結晶欠陥の密度は増加し、酸化膜耐圧特性も悪化してしまうことは明らかである。

【００２３】そこで、一つの仮説を立てた。ＦＰＤ、ＬＳＴＤ、ＣＯＰ等は欠陥といっても、原子レベルの点欠陥そのものを見ているのではなく、ある程度まとまった大きさのものを見ているのではないか。つまり、検出下限のようなものがあるのではないかと考えた。すなわち、結晶を従来の方法よりも急冷して欠陥のサイズをあるレベル以下に小さくしてしまえば、ＦＰＤ、ＬＳＴＤ、ＣＯＰ等のサイズも微小となり、その結果検出される密度も下がり、酸化膜耐圧特性を向上させることが可能ではないかと考えた。

【００２４】そこで、従来は実施していなかった急冷法も含めて１１５０～１０８０℃の温度域通過時間と欠陥密度及び酸化膜耐圧の調査を行うために、シリコン単結晶を育成の途中でシリコン溶融液から切り離した後、１１５０～１０８０℃の温度域通過速度を変化させ、シリコン単結晶の冷却速度を変える実験を行い、その結果を図１、図２に示した。なお、用いた結晶成長装置は、予め温度分布測定を行い、１１５０～１０８０℃の温度域が、約８ｃｍの長さがあることを確認した。

【００２５】図１は、結晶の１１５０～１０８０℃の温度域通過速度とＦＰＤ密度との関係を表し、通過速度が４ｍｍ／ｍｉｎ以下、つまり１１５０～１０８０℃の通過時間が２０分を境に２０分を超える領域（図１の左半分）では通過時間の短縮、すなわち通過速度が早くなるにつれてＦＰＤ密度は増加するが、反対に通過時間が２０分以下の領域（図１の右半分）では通過時間がさらに短縮される、すなわち通過速度が早くなるにつれてＦＰＤ密度が減少する領域を発見した。また、斜線で囲った

領域は、特にＦＰＤのサイズが小さく、密度も低く、今回の調査実験で発見した部分である。これは、極端な急冷がなされたため、欠陥のサイズが非常に小さく、検出下限を下まわるものが多くなるために起こる現象であると思われる。

【００２６】一方、図２は、結晶の急冷域通過速度と酸化膜耐圧特性の良品率との関係を表し、通過速度４ｍｍ／ｍｉｎを中心に低速側、高速側に変移するにつれて急速に向上していることが判る。したがって、１１５０～１０８０℃の温度域を２０分以下に急冷することによって、酸化膜耐圧特性を改善することが出来ることがわかる。

【００２７】また、さらに、シリコン単結晶の１１５０～１０８０℃温度域の通過速度を８ｍｍ／ｍｉｎ以上、つまり１１５０～１０８０℃の通過時間を１０分以下にすれば、シリコン単結晶中の欠陥のサイズはさらに小さくなり、ＦＰＤ密度も１００／ｃｍ^2 以下で、かつ、酸化膜耐圧特性の良品率も９０％以上と、酸化膜耐圧特性に優れた低欠陥結晶が得られることを発見した。

【００２８】この場合、単結晶を実際に４ｍｍ／ｍｉｎ以上あるいは８ｍｍ／ｍｉｎ以上で成長させるのは困難である場合もあるので、そのような場合は、結晶成長装置の炉内構造を調整して１１５０～１０８０℃の温度域に相当する部分の長さを２．０ｃｍ以下となるようにすればよい。２ｃｍ以下とすれば、例え通常の引上げ速度で結晶を成長させても、１１５０～１０８０℃の温度域の通過時間を２０分以下とすることが可能であり、所望結晶欠陥密度、欠陥サイズのものを得ることができる。

【００２９】さらに、本発明者等は、先に提案した特願平８－２６０２１号（特開平９－２０２６８４号）において、上記とは別の結晶熱履歴と結晶欠陥の関係を調査したところ、１２５０～１２００℃の温度帯の通過時間が、結晶欠陥核の形成に影響を及ぼしていることを発見した。この結果から１２５０～１２００℃の温度域に関しては、通過時間を２０分以下とすることによって、欠陥核の形成を抑制することができることを確認した。

【００３０】そこで、上記１１５０～１０８０℃の温度域を急冷する方法と、この１２５０～１２００℃の温度域を急冷する方法を組み合わせれば、欠陥核の形成が抑制されるため、より一層欠陥密度、欠陥サイズを小さくすることが可能となる。

【００３１】この場合も、結晶成長速度を高速とすることのみで１２５０～１２００℃の温度域を通過する時間を２０分以下としようとすると困難である場合もあるので、そのような場合は、１２５０～１２００℃の温度域に相当する部分の長さを２．０ｃｍ以下とするようにすればよい。２ｃｍ以下とすれば、例え通常の引上げ速度で結晶を成長させても、１２５０～１２００℃の温度域の通過時間を２０分以下とすることが可能であり、結晶欠陥核の形成を抑制し、所望結晶欠陥密度、欠陥サイズ

のものを得ることができる。

【００３２】

【発明の実施の形態】以下、本発明の実施の形態について、図面を参照しながら詳細に説明する。まず、本発明で使用するＣＺ法による急冷型単結晶引上げ装置の構成例を図３により説明する。図３に示すように、この急冷型単結晶引上げ装置３０は、引上げ室３１と、引上げ室３１中に設けられたルツボ３２と、ルツボ３２の周囲に配置されたヒータ３４と、ルツボ３２を回転させるルツボ保持軸３３及びその回転機構（図示せず）と、シリコンの種子結晶５を保持するシードチャック６と、シードチャック６を引上げるケーブル７と、ケーブル７を回転又は巻き取る巻取機構（図示せず）を備えて構成されている。ルツボ３２は、その内側のシリコン融液（湯）２を収容する側には石英ルツボが設けられ、その外側には黒鉛ルツボが設けられている。また、ヒータ３４の外側周囲には断熱材３５が配置されている。

【００３３】また、本発明の製造方法に関わる製造条件を設定するために、結晶の固液界面の外周から引上げ室の天井にかけて環状の固液界面断熱材９を設けている。この固液界面断熱材９は、その下端とシリコン融液２の湯面３との間隔を数ｃｍとして界面近傍の放熱を抑え、天井に向かっては成長単結晶１との空隙が連続的に大きくなるように厚さを薄くして急冷可能な構造にしている。また、ヒータ上部断熱材８を設けてヒータからの輻射熱を遮っている。別に、最近では引上げ室３１の水平方向の外側に、図示しない磁石を設置し、シリコン融液２に水平方向あるいは垂直方向等の磁場を印加することによって、融液の対流を抑制し、単結晶の安定成長をはかる、いわゆるＭＣＺ法が用いられることも多い。

【００３４】次に、上記の急冷型単結晶引上げ装置３０による単結晶育成方法について説明する。まず、ルツボ３２内でシリコンの高純度多結晶原料を融点（約１４２０°Ｃ）以上に加熱して融解する。次に、ケーブル７を巻き出すことにより融液２の表面略中心部に種子結晶５の先端を接触又は浸漬させる。その後、ルツボ保持軸３３を適宜の方向に回転させるとともに、ケーブル７を回転させながら巻き取り種子結晶５を引上げることにより、単結晶育成が開始される。以後、引上げ速度と温度を適切に調節することにより略円柱形状の単結晶棒１を得ることができる。

【００３５】この場合、本発明では、本発明の目的を達成するために特に重要であるのは、図３に示したように、引上げ室３１の湯面上の単結晶棒１の外周空間において、湯面近傍から引上げ室の天井にかけて環状の固液界面断熱材９を設けたことと、ヒータ３４の上にヒータ上部断熱材８を配置したことである。さらに、必要に応じてこの断熱材の上部に結晶を冷却する装置、例えば整流筒（図示せず）を設けて、これに上部より冷却ガスを吹きつけて結晶を冷却できるものとし、整流筒の下部に輻射熱反射板を取り付けた構造としてもよい。

【００３６】このように液面の直上の位置に所定の隙間を設けて断熱材を配置し、さらにこの断熱材の上部には成長単結晶との間に上部に向けて連続的に拡大する空間を設けた構造とすることによって、結晶成長界面近傍では輻射熱により保温効果が得られ、その上部は特定温度域が急冷構造となり、結晶の上部ではヒータ等からの輻射熱をカットできるので、結晶引上げ速度の制御と相まって本発明の製造条件を満足させることができる。また、結晶の冷却装置としては、前記筒状の整流筒とは別に、結晶の周囲を囲繞する空冷ダクトや水冷蛇管等を設けて所望の温度勾配を確保するようにしても良い。

【００３７】本発明で使用した急冷型単結晶引上げ装置と比較のために従来の徐冷型単結晶引上げ装置を図４に、従来の単結晶引上げ装置を図５に示した。基本的な構造については、本発明で使用した急冷型単結晶引上げ装置（図３参照）と同じであるが、固液界面断熱材及びヒータ上部断熱材の有無、断熱材の配置場所等が大きく異なっている。

【００３８】

【実施例】以下、本発明の実施形態を実施例を挙げて具体的に説明するが、本発明はこれらに限定されるものではない。

（実施例１）ＣＺ法で、直径１８インチの石英ルツボに、原料多結晶シリコン４０ｋｇをチャージし、直径６インチ、方位＜１００＞の結晶を図３に示したような急冷型の炉内構造を持つ単結晶製造装置により引上げた。１１５０～１０８０℃温度域通過時間：１２分、１１５０～１０８０℃温度域長さ：２０ｃｍ、１１５０～１０８０℃温度域通過速度（結晶引上げ速度）：１．６７ｍｍ／ｍｉｎに結晶成長条件を設定して単結晶を引上げた。

【００３９】ここで得られた単結晶棒から、ウエーハを切り出し、鏡面加工を施してシリコン単結晶の鏡面ウエーハを作製し、グローンイン欠陥および酸化膜耐圧特性（Ｃ－モード）を測定した。得られたシリコンウエーハのＦＰＤ、ＣＯＰ、ＴＺＤＢ（酸化膜耐圧特性良品率）の値を表１に示した。なお、酸化膜耐圧特性（Ｃ－モード）測定条件は、酸化膜厚：２５ｎｍ、測定電極：リンドープ・ポリシリコン、電極面積：８mm^2、判定電流：１ｍＡ／cm^2 とし、絶縁破壊電界が８ＭＶ／ｃｍ以上のものを良品と判定した。

【００４０】（実施例２）１２５０～１２００℃温度域通過時間１２分、１２５０～１２００℃温度域長さ２．０ｃｍ、１２５０～１２００℃温度域通過速度（結晶引上げ速度）：１．６７ｍｍ／ｍｉｎに引上げ条件を設定して引上げた以外は実施例１と同一装置を使用し、同一条件下に引上げた。その結果得られたシリコンウエーハのＦＰＤ、ＣＯＰ、ＴＺＤＢの値を表１に併記した。

【００４１】（比較例１）成長結晶の１１５０～１０８

０℃の温度域が徐冷型の炉内構造を持つ単結晶製造装置を使用して引上げ速度１．１ｍｍ／ｍｉｎで引上げた。その結果を表１に併記した。尚、図４にこの徐冷型単結晶引上げ装置４０を示した。基本的構構造については、本発明で使用した単結晶引上げ装置３０と同じであるが、１１５０～１０８０℃の温度域を徐冷させるため、ヒータ３４を取り巻く断熱材３５を上部に延長し、その上にカーボンリング１１を設置して、結晶表面からの輻射熱の放散を防いで徐冷化している。さらに、ヒータ３４を取り巻く断熱材３５の内、一部を切り欠き断裂部１０を設けて断熱材３５を上下に分割することによって融点から１２００℃までの高温域を急冷化させている。こ＊のような構造を持つ炉により、下記比較例２の従来の急冷法に比較して高温域の通過時間は減少し、１１５０～１０８０℃の温度域の通過時間を長くすることができるものである。

【００４２】（比較例２）従来の炉内構造を持つ単結晶引上げ装置５０（図５参照）を使用して、引上げ速度１．２５ｍｍ／ｍｉｎで引上げた以外は、特に冷却条件も設けずに単結晶を引き上げた。その結果を表１に併記した。

【００４３】

【表１】

項目 例No.	単結晶引上げ装置の型	ＦＰＤ［ケ／ｃｍ²］	ＴＺＤＢ（%）	ＣＯＰ（0.16μm）［ケ／ｃｍ²］
実施例１	1150～1080℃急冷型	≒２００	≒９０	≒１０
実施例２	1250～1200℃急冷型	≒３	≒９３	≒８
比較例１	1150～1080℃徐冷型	≒４００	≒８０	≒１００
比較例２	従来の急冷型	≒１０００	≒５０	≒１０

【００４４】なお、本発明は、上記実施形態に限定されれるものではない。上記実施形態は、例示であり、本発明の特許請求の範囲に記載された技術的思想と実質的に同一な構成を有し、同様な作用効果を奏するものは、いかなるものであっても本発明の技術的範囲に包含される。

【００４５】

【発明の効果】本発明によればＣＺ法によって製造されるシリコン単結晶の１１５０～１０８０℃の温度域，１２５０～１２００℃の温度域を急冷することによって、ＦＰＤ密度が１００［／ｃｍ²］以下でＣＯＰ密度が１０［／ｃｍ²］以下でかつ欠陥サイズが極めて小さく、かつ酸化膜耐圧特性が８０％以上の高品質のウエーハを製造することができる。しかも、結晶引上げ速度を低下させることなく高速を維持することができ、高品質の結晶を高生産性で生産することができる。

【図面の簡単な説明】

【図１】本発明において、結晶急冷温度域通過速度と得られたウエーハのＦＰＤ欠陥密度との関係を表すグラフである。

【図２】本発明において、結晶急冷温度域通過速度と得られたウエーハのＣモード酸化膜耐圧良品率との関係を表すグラフである。

【図３】本発明において使用された急冷型シリコン単結晶引上げ装置の説明図である。

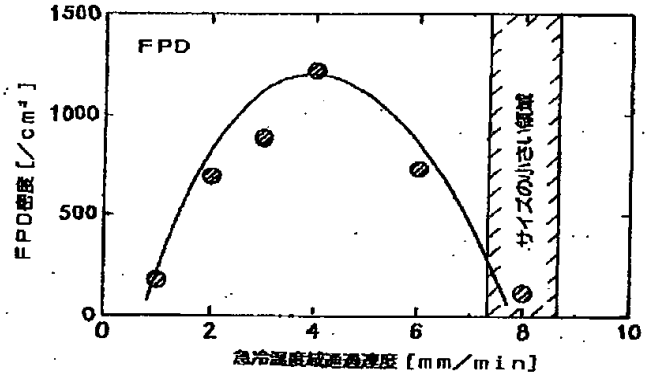
※【図４】従来の徐冷型シリコン単結晶引上げ装置の説明図である。

【図５】従来のシリコン単結晶引上げ装置の説明図である。

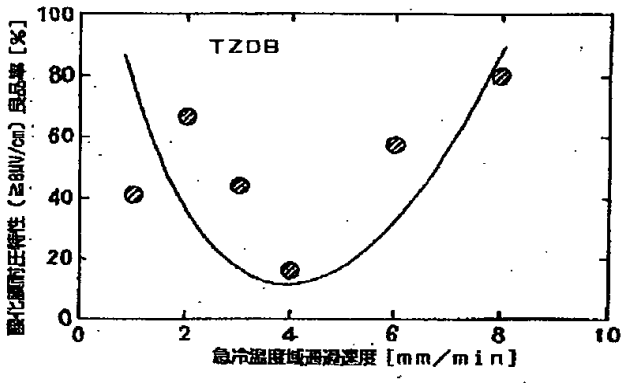
【符号の説明】

１…成長単結晶棒、
２…シリコン融液、
３…湯面、
４…固液界面、
５…種子結晶、
６…シードチャック、
７…ケーブル、
８…ヒータ上部断熱材、
９…固液界面断熱材、
１０…断裂部、
１１…カーボンリング、
３０…本発明に使用した急冷型単結晶引上げ装置、
３１…引上げ室、
３２…ルツボ、
３３…ルツボ保持軸、
３４…ヒータ、
３５…断熱材、
４０…従来の徐冷型単結晶引上げ装置、
５０…従来の急冷型単結晶引上げ装置。

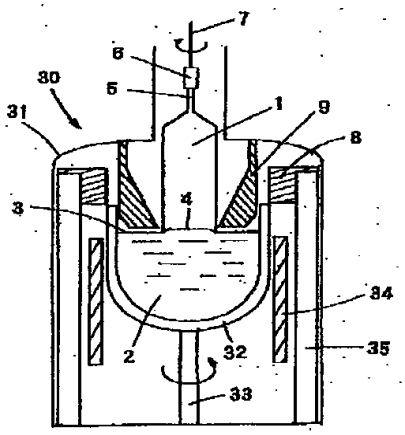
【図1】


FPD
FPD密度［/cm²］
急冷温度域通過速度［mm/min］
サイズの小さい領域
1500
1000
500
0
0
2
4
6
8
10

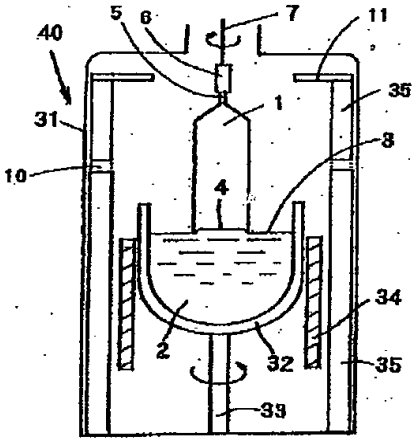
【図2】


TZDB
急冷温度域通過速度［mm/min］
100
80
60
40
20
0
0
2
4
6
8
10

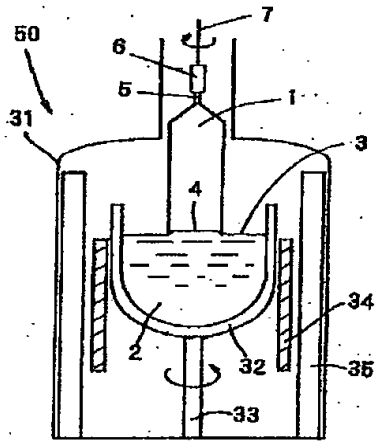
【図3】


7
6
5
30
31
1
9
8
3
4
34
2
32
35
33

【図4】


5
6
7
11
40
35
1
31
8
10
4
34
2
32
35
33

【図5】


7
50
6
5
1
31
3
4
34
2
32
35
33

フロントページの続き

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